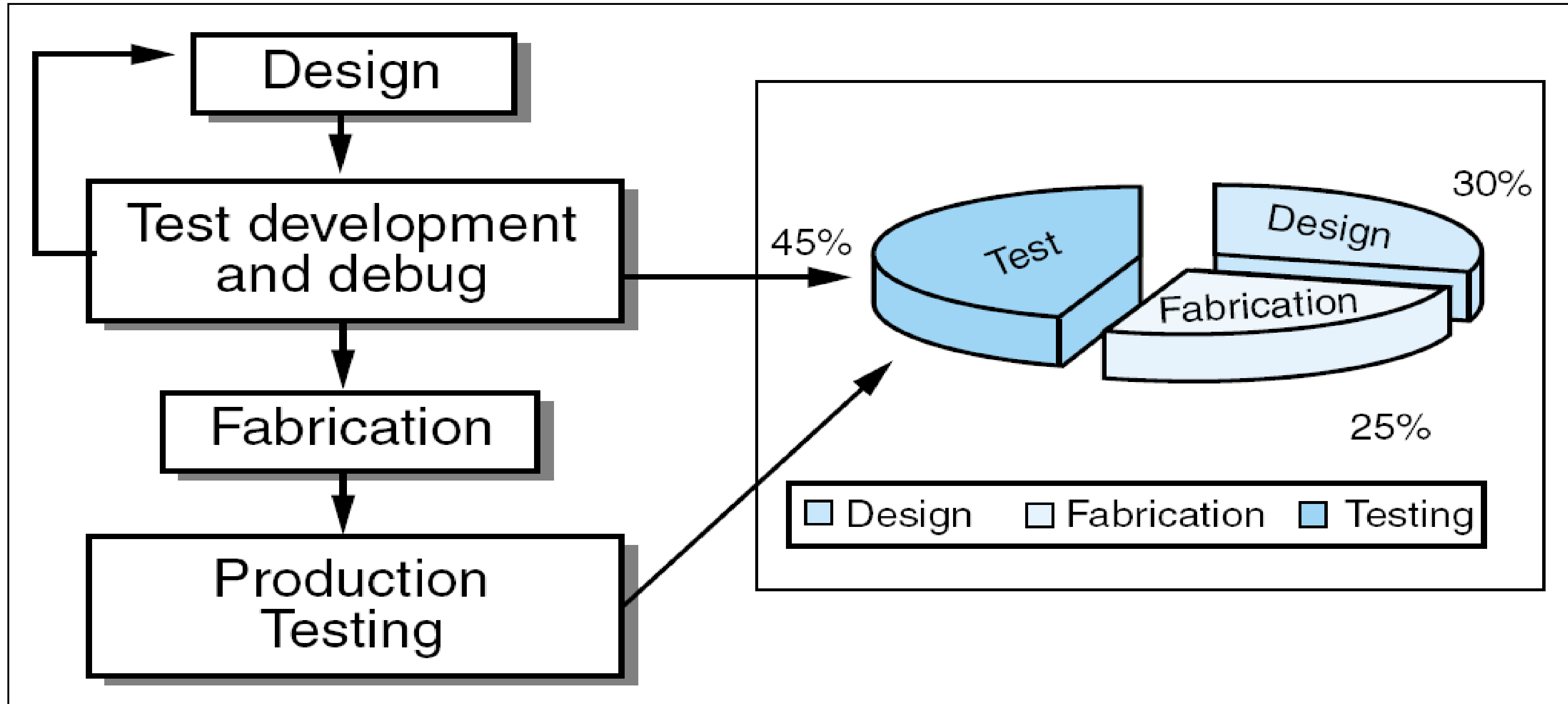
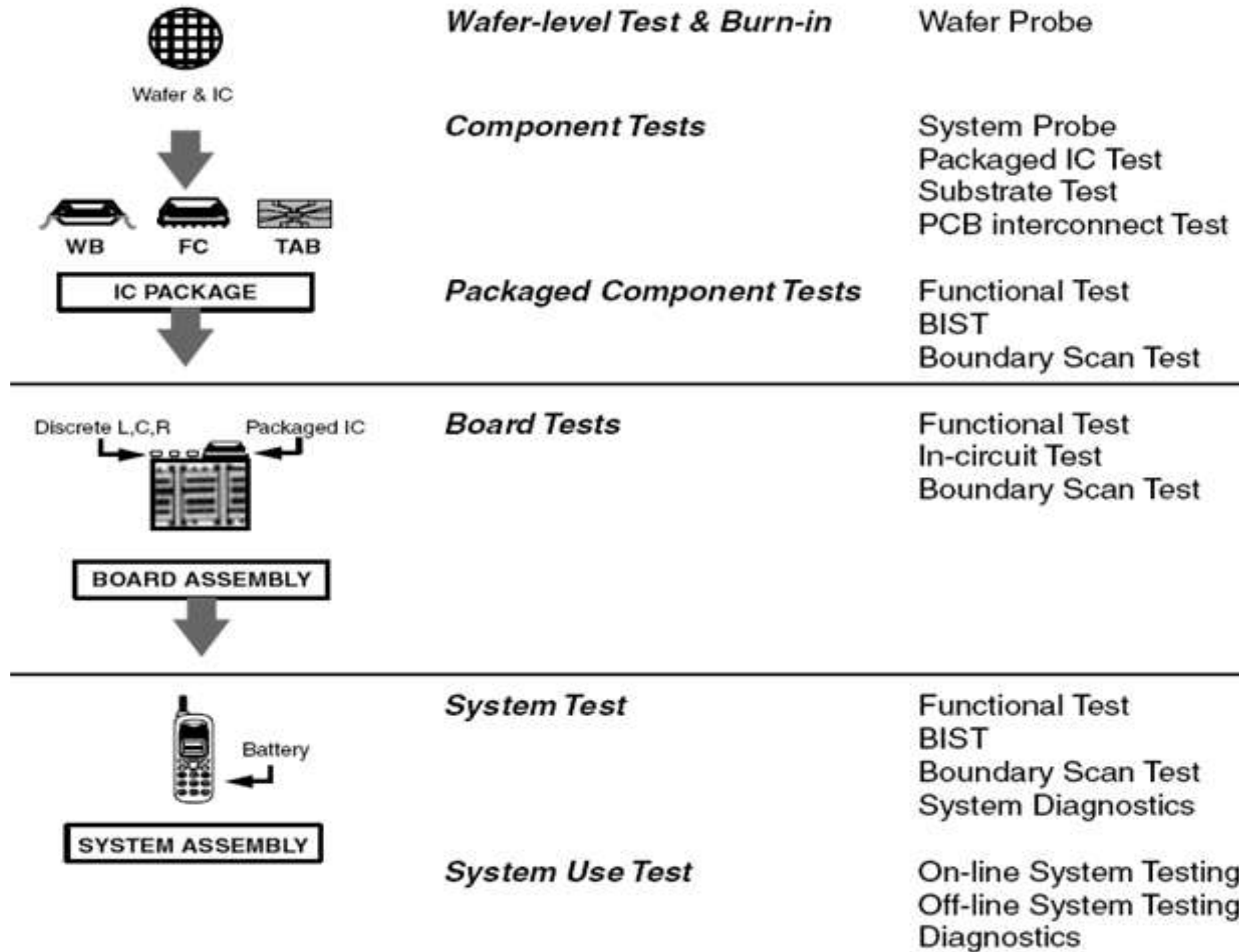
Electrical Testing

Electrical Testing

- Electrical testing is intended to guarantee that a given device is electrically functional before end-product use.
- Defects may be introduced at any point in the process



A Typical Testing Process



Common Faults

- Physical Faults:
  - Stuck-at-one or stuck-at-zero
  - Open faults
  - Latent faults
  - CMOS transistor stuck-on
  - Adjacent bridging
  - Partially conducting transistors
  - Resistive bridges
- Classified as permanent or transient

Defect level

$$DL = 1 - Y^{(1-C)}$$

DL: Defect Level is the fraction of all defect parts that pass testing

Y: Yield is the fraction of all parts that are good

C: Fault Coverage is the fraction of all possible faults detected by tests

- DL is usually specified in Defects Per Million

Testability

Testability depends on system

- Controllability: ease of stimulating the system
- Observability: ease of measuring responses

Designers should “design-for-testability” (DFT)

- Minor circuit modifications can greatly enhance controllability and observability
- Testability changes can ultimately lead to lower production costs
- Most popular DFT techniques are scan design and built-in-self-test (BIST)

Functional vs. Structural Testing

- Functional testing
  - Run the CUT through all intended functionality
  - Exhaustive
  - Completely impractical for any complex system
- Structural testing
  - Knowledge of the physical structure of the device is used to verify the CUT is constructed as designed
  - CUT is partitioned into simpler subcircuits
  - More efficient, but does not test actual functionality
  - Can miss "secondary" effects such as noise
- Test procedures usually include a combination

Testing

Quiescent Power Supply Current (IDDQ)

- Good at detecting CMOS stuck-on or bridging faults
- Power and an input signal is applied, any parts with excessive IDDQ may be damaged
- May supplant a later burn-in test

At-speed Testing

- Detects timing failures at intended clock rate
- Partially conducting transistors and resistive bridges will statistically affect chip timing

Testing

DC and AC Testing

DC tests involve measuring the system in a static state (i.e. no time varying inputs)

AC tests involving some time varying input and measure a time varying output

- For digital CUT AC tests would measure parameters such as set-up, hold, and propagation delay times

In general DC tests are easier

Typically only CUT that pass DC tests are subjected to AC testing

Testing

Pass and Fail Tests

Refers to any absolute test resulting in the scrapping of any CUT to fail requirements

Characterization Tests

A parameter is measured that determines the quality of a part.

Characterization tests are often used in early production to determine how to improve yield

Offline and Online Testing

Online testing refers to tests performed while the CUT is in use

Testing

Wafer Probe Testing

- Electrical tests are applied to the wafer
- Usually just establishes functionality
- Performance is determined after packaging
- Results are referred to as Known Good Die (KGD)

Burn-In

- CUT is subjected to elevated temperature and power supply voltages for and extended period of time
- Intended to reveal latent defects
- Burn-In is followed by electrical testing to identify failures

Higher Level Testing

Substrate Test

Interconnects on the substrate are tested for opens and shorts

Module Test

Testing of the assembled PCB as a unit

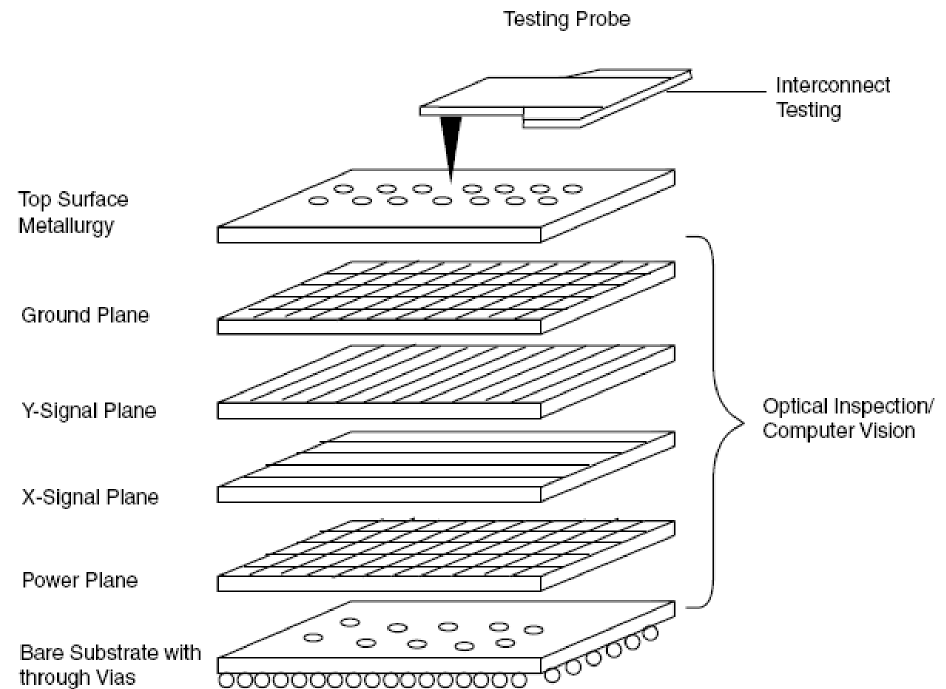
System

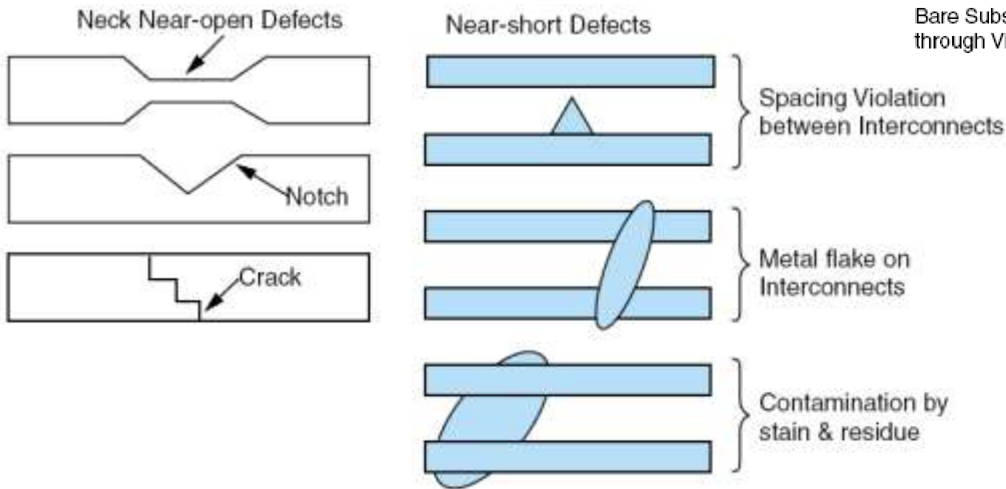
Entire assembled unit is tested for functinality

Interconnect Tests

Optical Inspection

During fabrication, every layer is optically inspected by computer





- Defects may still be introduced during assembly
- A substrate test must be applied to find latent defects

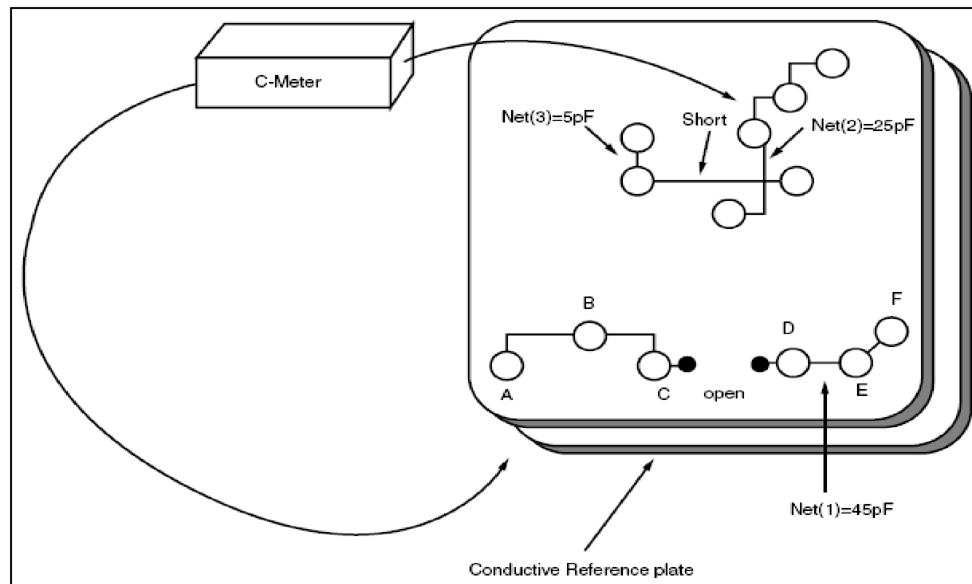
Capacitance Tests

- Capacitance testing can be used to find and identify latent failures

$$C_i = kA_i$$

k depends on spacing and dielectric

- An interconnect with an open will have a capacitance less than expected
- An interconnect with a short will have a capacitance higher than expected



Resistance Tests

- A small current is forced through an interconnect while the voltage across the interconnect is measured
- Can identify low-resistance opens and high-resistance shorts
- Always follows capacitance testing to verify faulty nets
- A “bed of nails” tester is used to minimize the need for mechanical movement of probes
- Alternative is the “flying probe” tester (30-100) times slower

Active Circuit Testing

steps are the key aspects of automatic test pattern generation (ATPG)

- Fault Models

  Purpose is to create a set of test patterns that detect as many manufacturing defects as possible

  Manufacturing defects classified in 3 groups

  - Functional defects that include circuitry opens and shorts
  - IDDQ defects that include CMOS stuck-on, CMOS stuck-open, and bridging
  - At high speed defects (slow transistors and resistive bridges)

  Most popular fault model assumes that each defect will cause a node to be "stuck" at a fixed voltage level (Single-stuck fault – SSF model).

  Assumes that only one fault exists at a time

  SSF makes the problem of enumerating faults and developing electrical tests tractable.

  SSF only tests for some of the possible faults so it is usually accompanied by a variety other tests.

Active Circuit Testing

- **Fault Set**

  In the structural fault model, the logic gates are assumed to be fault-free and only their interconnections are affected

  Fault set consists of all stuck-at-zero and stuck-at-one faults at all interconnects in a circuit.

  - significant number of faults that behave identically to other faults and can not be distinguished.
  - The fault identification process reduces the faults to one equivalent fault in a process know as fault collapsing.
  - The fault set can be further reduced by identifying those faults which dominate other faults.

Active Circuit Testing

- Test Pattern Generation and Fault Simulation

  Many automatic test pattern generators employ the algorithm shown below for efficient test generation

  Three most popular fault simulation algorithms employed are:

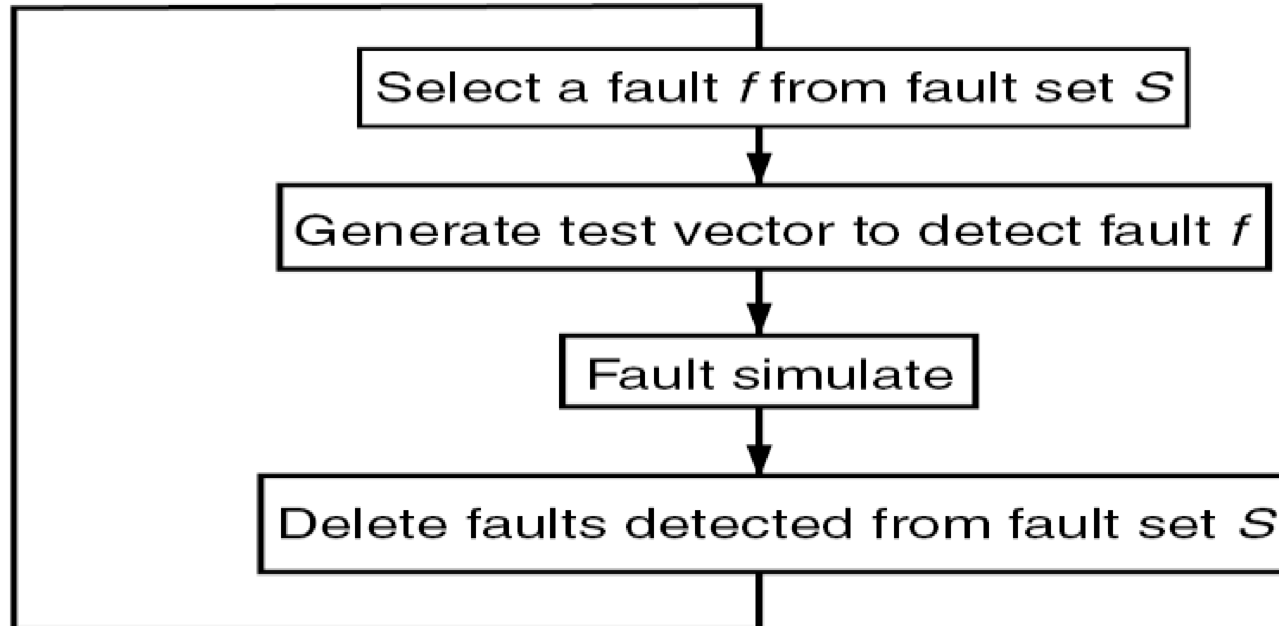
    - Parallel
    - Deductive
    - Concurrent Algorithms

  Test generation for a single fault involves two main steps

    - Activating the fault site
    - Propagating the faulty response to a primary output.

Active Circuit Testing

- Automatic test pattern generation flow.



Design for Testability: Scan Design

- Scan circuitry greatly enhances a design's testability, facilitates faster and improved test generation, and reduces external tester usage.
- **Internal Scan**

  Basic Idea is to control and observe the values in all the design's storage elements, so that all sequential circuit's test generation and fault simulation tasks are as simple as those of a combinational circuit

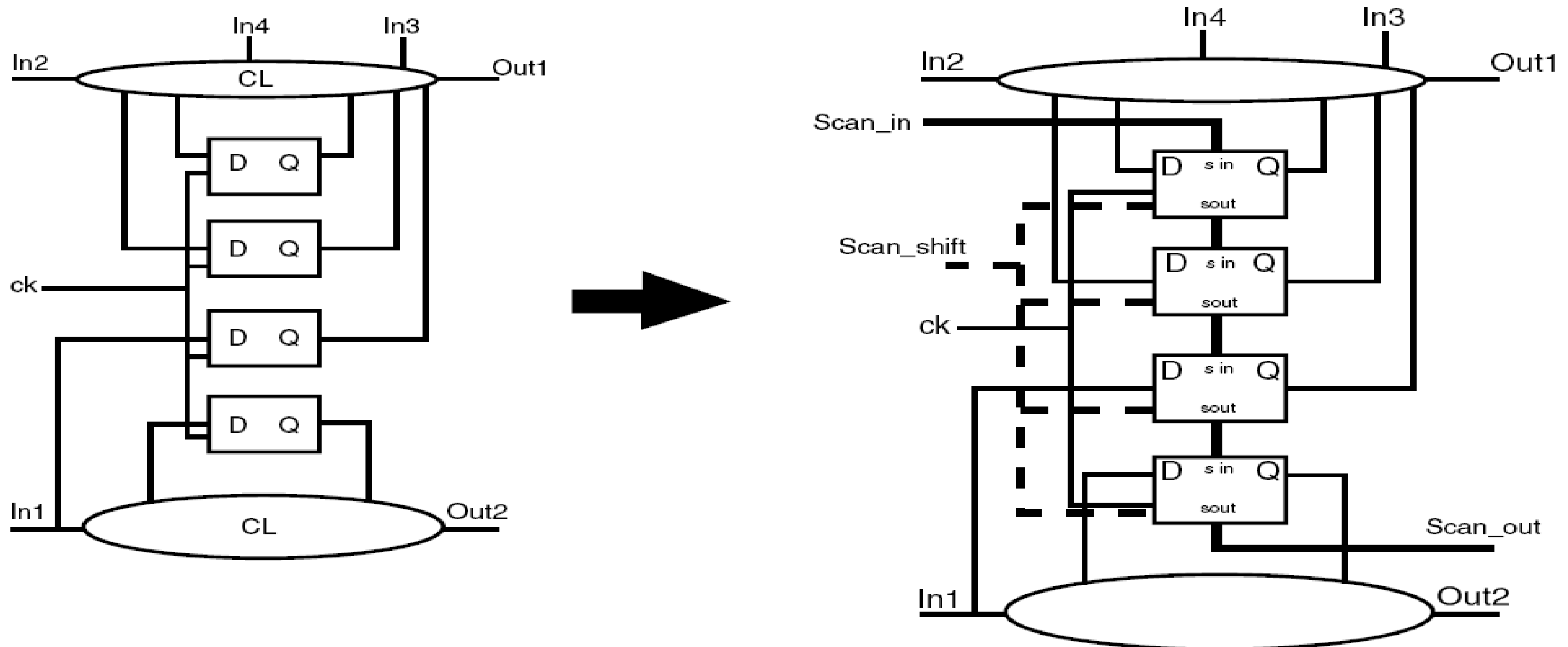
  Involves the internal modification of a design's circuitry to increase its testability.

  The goal of the scan design is to make a difficult-to-test sequential circuit behave like an easier-to-test combinational circuit.

  Operation as follows:
  - Shift data into scan chains
  - Apply stimulus to the primary inputs
  - Measure primary outputs
  - Pulse system clock to capture new values into scan cells
  - Scan data out to measure captured values while loading new value to chains

Design for Testability: Scan Design

- Circuit with both combinational and sequential scan elements



Scan Design

- **Boundary Scan**

  Boundary scan (JTAG) is a DFT (Design for Testability) technique that facilitates the testing of PWB and MCM interconnect and chips.

  Stitches the input and output ports together into a long scan path.

  It associates a memory cell with each input and output of a chip.

  These memory cells are connected serially to form a shift register.

Scan Design

- Boundary Scan

  The architectures also contains a four-port standard connection (the test access port – TAP)

  This provides access to this shift register and controls the various chip test modes.

  The TAP consists of four lines

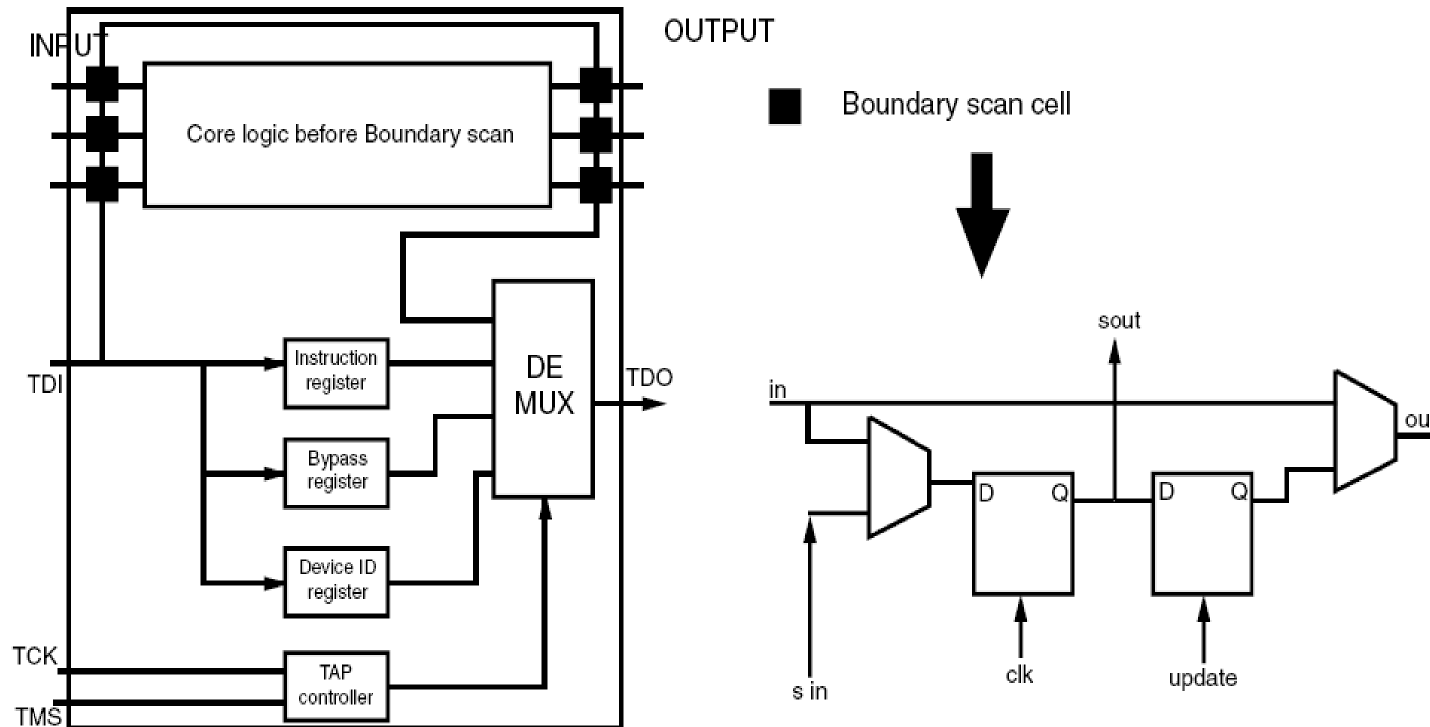
  - Test Clock (TCK)
  - Test Mode Select (TMS)
  - Test Data In (TDI)
  - Test Data Out (TDO)

  Two most popular modes are INTEST and EXTEST

  - EXTEST allows for off-chip circuitry and board-level interconnects.
  - BYPASS, IDCODE, SAMPLE, PRELOAD are other modes.

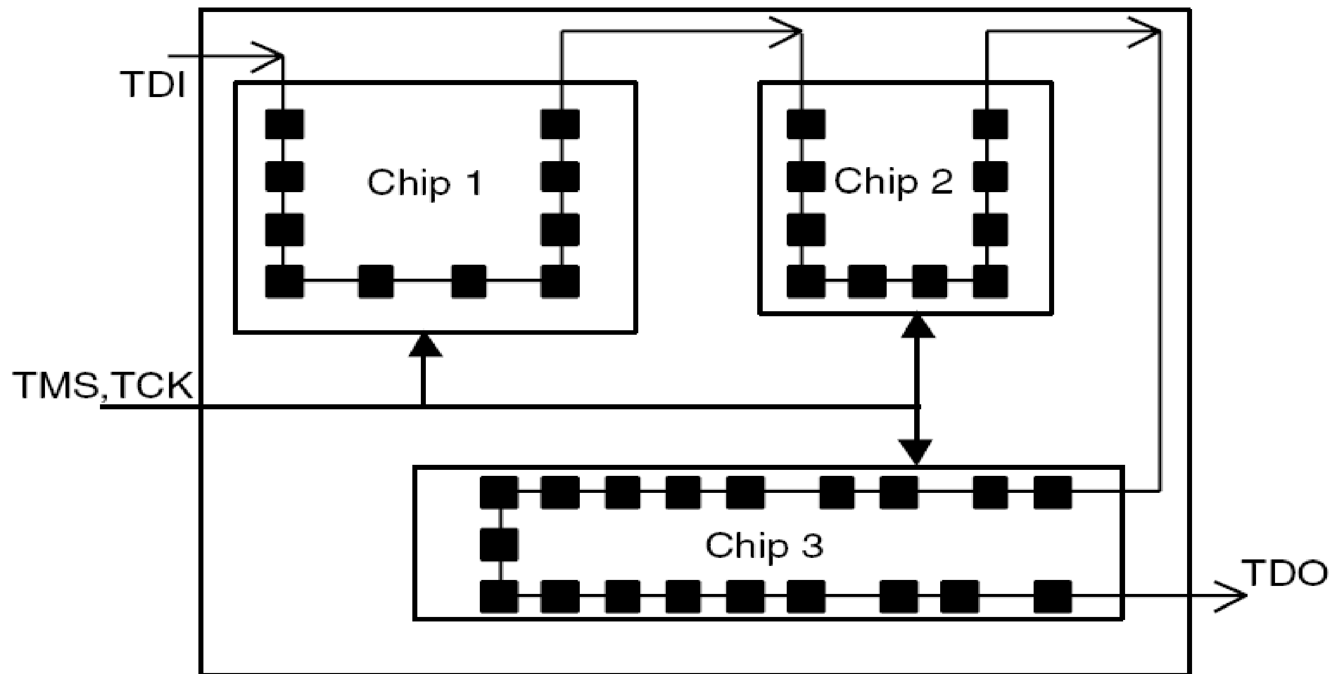
Scan Design

- Chip supporting boundary scan design and a boundary scan cell



Scan Design

- Boundary scan chain in a board with three chips



Built-in Self-Test (BIST)

- Built-in Self-Test (BIST)

  BIST is a structured DFT technique that places a device's testing function within the device itself.

  They generate test patters and compare output responses for a dedicated piece of circuitry

  BIST architecture for digital circuits require an addition of three hardware blocks.

  - A pattern generator
  - A response analyzer
  - A test Controller

  BIST is used extensively for at-speed testing of circuits

  Disadvantage is the use of silicon area to design test hardware

Future Trends

- Mixed Signal Tests
  - Digital logic, embedded dynamic RAM, and Analog blocks on a single IC
  - Each type requires different test sources and response analyzers
  - External test equipment performs these functions but these may involve three different external testers
- System-on-Chip (SOC) Test
  - Based on embedding cores to represent previously designed complex functional blocks.
  - IEEE P1500 standard for embedded-core test is under development
  - The goal is to ensure the test-friendliness of embedded cores from diverse vendors.